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Outpacing VME: OpenVPX fast-tracks technologies to the front lines

Advantages in SWaP, thermal management, and connectivity mean that OpenVPX's resultant rapid deployment is outrunning VME.

By 
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VPX is replacing VME. OpenVPX is that part of VPX that facilitates multivendor COTS system-level interoperability including modules, backplanes, and development chassis. Since embedded defense systems must often be developed and deployed rapidly, it is very important that potential conflicts are eliminated as quickly as possible during the design phase.

VME has long been used in mission-critical embedded systems. However, its VPX (VITA 46) progeny surpasses VME in bandwidth and power. But VPX designers soon found that VPX yielded its share of system-level interoperability issues: Multiple vendors' boards and components were often incompatible within the larger system design, presenting a major obstacle to VPX system development. The answer: OpenVPX (VITA 65), a leading system architecture standard in field-deployed, mission-critical embedded systems.

OpenVPX's goal is to provide a framework for system-level interoperability for COTS-based VPX Line Replaceable Units (LRUs). LRUs' main plus is that they are Two-Level Maintenance (2LM) compatible. The ultimate goal of two-level maintenance in all complex defense systems, including OpenVPX, is to enable a field technician without special maintenance tools to quickly identify a faulty board and swap it in a harsh and hostile environment – and therefore quickly return the system to operation.

The need for speed is also relevant to the OpenVPX design phase. Since embedded defense systems must often be developed and deployed rapidly, it is very important that potential conflicts between the various profiles are eliminated as quickly as possible. SWaP and thermal management, along with other requirements, must be resolved faster so that advanced capabilities can be swiftly engaged.

Accordingly, OpenVPX's proven field-deployed readiness and advanced systems design flexibility hasten the delivery of next-generation customizable COTS solutions to the front lines, today and tomorrow – and at a rapid pace. The following discussion examines VME and OpenVPX pertaining to:

1. SWaP and thermal management

2. Technical considerations for connectors and backplanes

SWaP and thermal management

Current and future embedded processors are pushing and exceeding the once prime-time VME64x 35 watts/slot at +12 V limit. Processor core densities and the number of cores on a chip are increasing the input power required by processor boards. Even as the power efficiency of processor technology increases, demand for increased operation rates and complexity will probably take up the slack in order to more rapidly increase deployment of OpenVPX-based technologies to the warfighter. A look at SWaP and thermal management considerations will lend insight.

Currently, OpenVPX uses 3U (100 mm x 160 mm) and 6U (233 mm x 160 mm) form factors. Since more applications are moving to the lighter, smaller 3U form factor, heat management has become more important than ever, which, of course, ties into power considerations. SWaP is not specified by VME or VPX, but OpenVPX is defined to supply 120 W at 5 V and 383 W at 12 V. The challenge is that this increased power creates heat management issues.

While OpenVPX does not consider specific temperature range or heat-flow-rate cooling strategies, the dimensions of board features such as side rail wedge mounts to facilitate conduction cooling are specified. Rugged and serviceable OpenVPX COTS is standardized in VITA 46 and VITA 48 (VPX-REDI). Dimensional specifications for cooling are given in VITA 48.1 for convection, VITA 48.2 for conduction, as well as VITA 48.3 for liquid. Covering all cooling methods in one standard enables board manufacturers to offer each board design with various cooling options.

Although all forms of heat management are supported by OpenVPX, conduction cooling is becoming the method of choice for ruggedized military and aerospace applications. Air is often contaminated or unavailable, and convection is often inadequate. Forced-air and liquid cooling require fans and pumps. Mechanical devices fail quicker than electronics and can severely reduce MTBF below 200,000 hours, which is often the minimum required for mission-critical systems. The development of heat pipes that can carry more than 150 times the heat flow per volume than aluminum is increasing the popularity of conduction-cooled OpenVPX thermal management systems.

Making the connection

OpenVPX connectors are a significant advance over VME alternatives. They provide greater bandwidth, inlet power, number of pins, and serviceability (Table 1). OpenVPX connectors also facilitate system-level development of VPX LRUs, to speed deployment and help maintain OpenVPX technologies' field readiness. The MultiGig RT family of connectors, for example, provides much higher bandwidth, pin density, and mission-critical ruggedness than VME64x's DIN 41612 connectors.

	VME64x	OpenVPX (VITA 65)
Bus characteristics		
Common bus used	VMEbus	PCI Express (PCIe)
Typicall bus bandwidth	Supports 80 MBps for standard 64-bit VME, up to 320 MBps for the 2eSST standard	PCIe v2.x = 500 MBps per lane, 16 lanes (PCIe v2.x = 8 GBps)
Bus minimum pin count	106 (approx.)	4 = 1 lane
Minimum bus width	64 bit	1 lanes (1 TX diff. pair + 1 RX diff. pair)
Standard max bus width	64 bit	16 lanes (PCIe v2.x = 8 GBps)
Bus Size Variation	64 bit	1,2,4,8,16 lane variations
Additional commonly available bus interface	100 Mb/1 GbE	Serial RapidIO/10 GbE
Bus links configurable by FMM	No	Yes
User-defined connector features		
Common user I/O pin counts	205	6U = 360 , 3U = 108 (varies by module profile type - important to review card selected)
Pin arrangement in connector	Low-speed pin construction with minimal GND shielding	Integrated controlled impedance differential pair conductors with GND shielding between each pair for improved signal integrity
User I/O variation above standard pin count	No	Might increase depending on bus width implementation
Different module interface and user I/O "profiles"	No	Yes - Important to evaluate profile compatibility
Connector variations	No	Differential pair or single-ended pin arrangements
I/O routable by FMM	No	Yes
Other feature sets		
Thermal models	Air/conduction cooled	Air/conduction/liquid cooled
Standard form factors	6U	6U and 3U
PMC/XMC capable	Yes (XMC support varies)	Yes
Standard voltages	+3.3V, +5V,+12V,-12V,Optional (-V1,+V1,-V2, +V2)	3U = (VS2)+3.3V,(VS3) +5V,(VS1) +12V, Aux+12V,Aux-12V, Aux+3.3V
		6U = (VS2)+12V,(VS3) +5V,(VS1) +12V, Aux+12V,Aux-12V, Aux+3.3V

Table 1: A comparison of VME64x and OpenVPX (VITA 65)

(click graphic to zoom by 1.9x)

Specifically, 3U OpenVPX boards have three MultiGig RT2 connectors (P0 – P2):

- P0 has 56 pins for power, addressing, system management, and other utility signals.
- P1/P2 have 112 pins each that can be used as differential pairs or as single-ended conductors.

The 6U boards have seven connectors. P3 through P6 can be used for differential pairs or single-ended signals, with one row of P3 through P6 reserved for single-ended signals. Other signals requiring coax or fiber optics can be connected through P5 or P6. Currently, coax and fiber optics for 3U boards are not prescribed by OpenVPX. However, they can be custom connected from the front panel.

The MultiGig RT connector's ruggedness facilitates military 2LM. It permits boards to be removed and inserted by reasonable manual force from front handles. The MultiGig RT connector has been tested for thermal and mechanical shock, vibration, and contaminants. Through severe testing, pin contact resistance remains low. The MultiGig RT connector has electrically grounded blades adjacent to sensitive recessed pins, making it virtually impossible to touch a pin without being grounded. This eliminates the possibility of electrostatic damage through the connector. The covers on both sides protect the board from electrostatic damage and debris.

Backplane to the future

If the backplane can be chosen quickly and well, OpenVPX systems can be deployed faster. And historically, high-speed switched serial fabric presented the most compelling demand for a new backplane architecture. The bandwidth of the OpenVPX backplane is greatly improved over the VMEbus 40-60 MBps range. The OpenVPX backplane can be configured into many network topologies such as mesh, star, dual-star, ring, or daisy chain. These networks permit multiple signals to be routed such that several cards can talk to each other simultaneously, achieving an aggregate bandwidth well over 100 GBps.

The OpenVPX backplane profile supports 10 GbE, PCI Express, Serial RapidIO, and SATA for nonvolatile memory. New revisions of these standards will push the limits of differential copper pairs; OpenVPX provides for coax and fiber-optic connections for higher-speed data and other signal formats.

OpenVPX COTS backplanes can also provide more options if problems arise later in the design or manufacturing phase. For example, a multi-Gigahertz tested Fabric Mapping Module (FMM) can connect to the backplane and modify its topology, making it more flexible. It provides quick-turn backplane customization, thus eliminating interconnect conflicts. Dawn VME Products' FMMs use BGA (Ball Grid Array) substrate technology as a "micro overlay," similar in function to overlays used on VME backplanes except that FMMs can be used on VPX backplanes and are tuned for high-speed signal transmission (Figure 1). They can:

- Directly connect PCI Express or SerialRapidIO to multiple cards or cards and switches
- Link SATA from a CPU card to a Solid State Drive (SSD) carrier
- Enable XMC cards to talk to other XMC cards

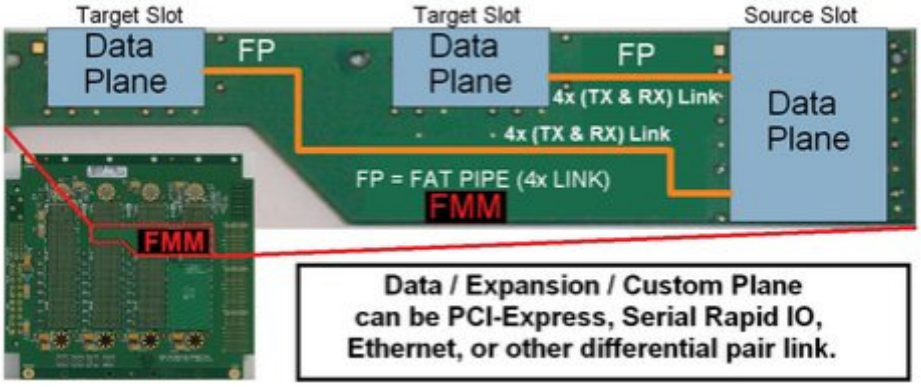

Figure 1: Expansion diagram of FMM micro overlay with two fat pipe PCI Express links

(click graphic to zoom by 1.9x)

Dawn engineers have successfully used Fabric Mapping Modules to solve many OpenVPX application problems in the design phase.

Designing with OpenVPX for rapid deployment

At one time, VME was found in military systems aplenty. But modern weapon and other embedded defense systems are becoming more modular and much simpler and faster to service using LRUs. Thus VME is being outpaced. OpenVPX, on the other hand, facilitates VPX LRU development by providing system-level, multivendor interoperability.

Since these embedded defense systems and VPX LRUs must often be developed and deployed rapidly, it is very important that potential conflicts between various profiles are eliminated as quickly as possible during the OpenVPX design phase. SWaP and thermal management, in addition to connector and backplane technical considerations, must be addressed and resolved faster so that advanced capabilities can be swiftly engaged to the warfighter. CS

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